WEST Search History

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☐	L11	l1.ab. and L8	2
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☐	L7	l3.ab.	3
☐	L6	(computer near5 (real adj time)) same (deep adj sleep)	2
☐	L5	((deep adj sleep) near2 (mode or state)) same (computer near5 process$4)	2
☐	L4	((deep adj sleep) near2 (mode or state)) same computer	23
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☐	L1	(real adj time) same (buffer$4 or queu$4 or fifo)	11104

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L18: Entry 6 of 22 File: USPT Apr 9, 2002

DOCUMENT-IDENTIFIER: US 6370564 B2
** See image for Certificate of Correction **
TITLE: Computer system architecture and method for multi-user, real-time applications

Brief Summary Text (3):
There exist various computer system architectures that provide multiple user access to computer applications. FIGS. 1-5 illustrate such known architectures and will be described in detail. The advantages and disadvantages of these known architectures will be described with reference to their running real-time computer applications and, more particularly, game applications. Of course, other real-time applications can be processed.

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L15: Entry 1 of 5 File: USPT Apr 22, 1986

DOCUMENT-IDENTIFIER: US 4584605 A
TITLE: Digital hysteresis for video measurement and processing system

Brief Summary Text (5):
Although offering a substantial amount of quantitive information regarding the image scanned by the video camera, the frame grabbing technique suffers as an inherently slow and expensive approach to video data acquisition. The drawback is largely attributable to the requirement to process approximately 10.sub.5 pixels per frame of video information. Relatively sophisticated and commensurately expensive hardware is required to digitally encode the analog signal representing the brightness level of each pixel and thereafter transfer into memory the information so encoded. Furthermore, the technique necessitates the use of a relatively powerful, in terms of both storage as well as a computational capacity, computing mechanism in order to process the video data so acquired in anything approaching real time applications.

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L4: Entry 8 of 23 File: USPT Feb 12, 2002

DOCUMENT-IDENTIFIER: US 6347379 B1
TITLE: Reducing power consumption of an electronic device

Detailed Description Text (36):
There are at least two ways to prevent glitching of the power good signal during the modified deep sleep state. The internal power good may be gated by a signal which is the logical AND of a signal indicating whether the computer has a modified deep sleep state and a signal indicating that the modified deep sleep state has been entered.

L4: Entry 2 of 23 File: USPT Oct 12, 2004

DOCUMENT-IDENTIFIER: US 6804792 B2
TITLE: Computer power management with converter for changing generated power mode commands for external devices

Brief Summary Text (6):
Standards for the power saving function include the International Energy Star standard which defines that a computer must comprise a function capable of activating the low-power mode and deep sleep mode of a display. The low-power mode is the first low-power state which is automatically activated after the computer does not operate for the first predetermined time. The deep sleep mode is the second low-power state which is automatically activated when the computer does not operate for the second predetermined time. According to this standard, the shift time for activating the low-power mode must be set within 30 min, and the shift time must be set to activate the deep sleep mode within 70 min. Further, the total of the shift times to the low-power mode and deep sleep mode must fall within 70 min. Note that the shift time is changeable by the user.

Brief Summary Text (7):
For example, if the computer does not operate for a predetermined time or more set by the user, an operating system (to be simply referred to as an OS hereinafter) generates the first operation mode signal for shifting to a standby state (corresponding to the low-power mode) in which the screen display is turned off. Further, if the computer does not operate for another predetermined time or more set by the user, the OS outputs the second operation mode signal for shifting to a power-off state (corresponding to the deep sleep mode). The BIOS receives these mode signals, and controls the display controller to control the operation state of the display.

Brief Summary Text (11):
Most of the OSs of conventional computer systems first output a standby mode signal when a computer does not operate for a predetermined time, and then output a deep sleep mode signal to set the power-off state when the computer does not operate for another predetermined time.

Brief Summary Text (14):
Along with upgrading (function advance) of an OS, the upgraded version of the above-mentioned OS (if the non-operation state continues for a predetermined time, the OS first outputs a low-power mode signal, and if the non-operation state further continues, outputs a deep sleep mode signal) can be used as a server OS. When the server OS, which immediately shifts to the power-off state in non-operation, is upgraded, the display device of a client is not immediately set to the power-off state but is temporarily set to the standby state. A client user who does not know the change of the OS or forgets it may mistake this state for a malfunction of the computer, and may be confused. Even a user who knows the change of the OS may feel unnatural if display operation changes.

L5: Entry 1 of 2 File: USPT Jan 11, 2000

DOCUMENT-IDENTIFIER: US 6014751 A
** See image for Certificate of Correction **
TITLE: Method and apparatus for maintaining cache coherency in an integrated circuit operating in a low power state

Detailed Description Text (7):
Referring to FIG. 3, there is shown a state diagram 100 illustrating the various clock states of a processor according to one embodiment of the invention. The illustrated clock states facilitate power control of a processor in both Uni-Processor (UP) mobile computer systems, and Symmetrical Multi-Processor (SMP) detktop and server computer systems. Six distinct clock states are illustrated, namely a Clock Running state 102, a Stop Grant state 104, an Auto Halt State 106, a Quick Start state 108, a Sleep state 110 and a Deep Sleep state 112. In the clock states 102 to 108, shown above the line 114, some degree of processor bus snooping for the purposes of cache coherency is facilitated, while in the states 110 and 112 below the line 114, the processor bus is not snooped. The distinction between the various clock states will now be described in further detail.

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L6: Entry 1 of 2 File: USPT Oct 31, 2000

DOCUMENT-IDENTIFIER: US 6138516 A
TITLE: Low-power shock detector and detection method

Detailed Description Text (14):
The data logger 90 is adapted to store the time measurement data and acts as a means for storing the time that the conditioned electrical vibration signal is in the high voltage state. Many commercially available data acquisition units, or data loggers 90, are able to count pulses on digital lines while in deep sleep mode. The data logger 90 may then be preprogrammed to awake at scheduled times to analyze and record the previously acquired data. Thus, determining the time spent in the high voltage state and analyzing this data may be done at very low levels of power consumption. The data logger 90 also has the capability of performing computational analysis. For example, the data logger 90 determines whether a critical shock event has occurred. The data logger 90 performs the calculations in real time, as the event occurs. However, as the data logger 90 has limited storage and computational resources, the computations that do not require real-time analysis are preferably allocated to a remote computer 110, described below.

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L19: Entry 1 of 6 File: USPT Jan 6, 2004

DOCUMENT-IDENTIFIER: US 6675070 B2
TITLE: Automation equipment control system

Detailed Description Text (20):
Real-time computer subsystem 16 includes a robot move module 32, a move command data buffer 34, kinematic models 36, servo control algorithms 38, and watchdog intercommunication code segments 40. Real-time subsystem 16 also includes I/O hardware and software drivers to provide an operable link to the positioning related electronics of robot 4. Represented by block 42 in FIG. 1 are the hardware and software components necessary for receiving and translating robot feedback signals 44 into computer data feedback signals 46. Likewise, block 48 represents the components necessary for converting computer data setpoints 50 into actuator-appropriate activation signals 52.

Detailed Description Text (63):
Each automation device 204A and 204B is served by separate real-time computer subsystems 216A and 216B, respectively. Real-time subsystem 216A is customized for control of robot 204A. Subsystem 216A includes hardware and software interface components 248A to transfer activation signal setpoints 250A to robot 204A actuators, interface components 242A to receive and translate position feedback signals 244A and interface components 245A for communication with end effector 209A. Also installed on real-time subsystem 216A is a move command data buffer 234A for receiving move commands 226A from general purpose computer 214, a move module software process 232A for translating move commands into activation signal setpoints 250A and watchdog communication code segments 240A to shutdown robot 204A in the event of a fault in general purpose computer 214.

Detailed Description Text (65):
It is a feature of the present invention that the interface hardware (e.g. 245A/B and 248A/B) and the software modules making up the real-time subsystems can be customized according to the selected automation equipment to be controlled, while the software modules resident on the general purpose computer (e.g. operator interface 220) can accommodate differing automation devices and their related electromechanical configurations. For example, industrial robot 204A has at least four revolute mechanical joints and corresponding actuators, while machining center 204B has a lower number of linear joints. Therefore, milling center subsystem 216B is customized with relatively less complex interface connections, than the connections required by subsystem 216A for robot 204A. Furthermore, the kinematic model present in move module 232B of subsystem 216B for machining center 204B can be relatively less complex than those kinematic models present in move module 232A of subsystem 216A.

Detailed Description Text (71):
Although represented in FIG. 9 as two separate blocks 222A and 222B, the watch dog intercommunication function between general purpose computer 214 and each real-time subsystem 216A and 216B preferably relies on the same operating code segments. The watchdog code segments in general purpose computer 214 set separate activity software switches for each subsystem 216A and 216B. If one or more critical software processes fail to execute, neither the activity software switch for subsystem 216A nor the activity software switch for subsystem 216B will be set to

L19: Entry 5 of 6 File: USPT Sep 7, 1999

DOCUMENT-IDENTIFIER: US 5948089 A
TITLE: Fully-pipelined fixed-latency communications system with a real time dynamic bandwidth allocation

Detailed Description Text (54):
The requirement for frequency decoupling is primarily based on the rich variety of systems that can benefit from this approach. One example system is a wireless personal communicator, which requires fixed-performance real-time subsystems (to implement the wireless communications) along with low-performance, computer-derived subsystems such as a microcontroller core, embedded memory, keypad input and liquid crystal display (LCD) output. Key design goals for the communicator are to provide reliable communications and as many features as possible (implemented in software on the microcontroller) at low power. A second exemplary system is a set-top box for receiving digital satellite television broadcasts. The set-top box design requires much higher bit-rate data communications and higher computational performance to decompress the video and audio data, and must guarantee performance across the entire system to avoid dropping frames. A third example is an Asynchronous Transfer Mode (ATM) switch. The switch design likely needs a central processing unit (CPU) only to monitor performance and provide diagnostics; the normal operation would involve switching packets between identical subsystems across the shared interconnect. As in most circuit switching applications, performance guarantees are critical to proper operation of the ATM switch.

L18: Entry 4 of 22 File: USPT Jun 24, 2003

DOCUMENT-IDENTIFIER: US 6584489 B1

**** See image for Certificate of Correction ****

TITLE: Method and system for scheduling the use of a computer system resource using a resource planner and a resource provider

Detailed Description Text (14):

Although FIG. 1 depicts a single processor computer system for practicing the preferred embodiment to the present invention, those skilled in the art will appreciate that the present invention may also be practiced in distributed environments. Moreover, the present invention may be practiced in computer systems that have configurations that differ from that depicted in FIG. 1. The depiction in FIG. 1 of the computer system 10 is intended to be merely illustrative and not limiting of the present invention. For example, more than two real-time application programs may be concurrently running on the computer system in some alternative embodiments.

CLAIMS:

9. A computer system for running real-time applications programs, the computer system comprising: one or more resources; an application programming interface usable by real-time applications programs to request use of resources subject to time constraints; a resource planner for allocating resources in response to requests to use resources received by the application programming interface from real-time applications programs; and a scheduler for scheduling the use of resources requested by the real-time applications programs and allocated by the resource planner.

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L22: Entry 4 of 9 File: USPT Dec 31, 1996

DOCUMENT-IDENTIFIER: US 5590286 A
TITLE: Method and apparatus for the pipelining of data during direct memory accesses

Detailed Description Text (4):
A high speed memory bus 45 is also coupled to the CPU 10 to provide a high speed data path between memory and the CPU. The memory interface 140 communicates data between main memory 40 and the processor 10, as controlled by the memory management unit (MMU) 135. In the embodiment described, memory 40 is a random access memory which can function as a DMA (Direct Memory Access) device. The external device 30 is a bus master device, such as an Ethernet controller, SCSI controller or intelligent video frame buffer, through which direct memory access operations to the memory 40 are performed. An external bus controller 150, communicates data between the processor 10 and the external bus 20. The external bus 20 operates at a slower clock speed, for example, three to five times slower than the memory bus of the processor unit 10. The slower clock speed is taken advantage of by pipelining the data transfers to be performed between the memory 40 and the processor unit 10.

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